Attorney Docket No. B-3964 618029-8

PATENT

AF/2815

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Lap-Wai Chow et al.	On Appeal to the Board of Appeals
Patent Application No.: 09/768,904	
Filed: January 24, 2001	Group Art Unit: 2815
	Examiner: NGUYEN, JOSEPH H
For: "INTEGRATED CIRCUITS PROTECTED AGAINST REVERSE ENGINEERING AND METHOD FOR FABRICATING THE SAME USING AS APPARENT METAL CONTACT LINE TERMINATING ON FIELD OXIDE"	Date: February 24, 2005

BRIEF ON APPEAL

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from the Final rejection, dated July 15, 2004, for the above identified patent application. The Applicants submit that this Appeal Brief is being timely filed, since the notice of Appeal was filed on January 11, 2005.

REAL PARTY IN INTEREST

The present application has been assigned to HRL Laboratories, LLC of Malibu, CA.

STATUS OF CLAIMS

Claims 1-20 and 23-24 are currently pending and are reproduced in the accompanying appendix. Claims 9-16, 19-20 are the subject of this Appeal. The Examiner has allowed claims 1-8 and 17-18. Claims 23-24 were found to be patentable if rewritten in independent form including all of the limitations of the base claim. Claims 21-22 have been canceled.

STATUS OF AMENDMENTS

No Amendment After Final Rejection has been entered.

SUMMARY OF INVENTION

The invention described and claimed in the present application relates to the semiconductor devices containing metal traces leading to field oxide layers to prevent and/or thwart reverse engineering of the semiconductor device and the process or method for fabricating such devices.

In order to avoid the expenses of designing and developing semiconductor integrated circuits, some developers practice reverse engineering by disassembling products manufactured by somebody else and closely examining them to determine the physical structure of the integrated circuits, followed by copying the products. Such practices harm the true developer of the product and impair its competitiveness in the market-place, because the developer had to expend significant resources for the development, while the reverse engineer did not.

Usual practice of reverse engineering is to try to determine a basic structure of an integrated circuit by identifying metal patterns in the higher level metal layers in the circuit. Metals on these layers route the electric signals between circuit blocks. Once a basic circuit function is determined, rather than look at each next transistor pair, the reverse engineer will utilize the

similarity in the upper metal patterns and assume each circuit section showing that pattern is the same. Hence, there is a need for a defensive method which can help to provide protection against the reverse engineering of semiconductor circuits.

According to the present disclosure, the reverse engineer is forced to examine every connection of every transistor pair in an integrated circuit which would require a significant amount of time and money thereby making the reverse engineering of the integrated circuit time and cost prohibitive and leading to *de facto* protection against reverse engineering.

A first embodiment of a semiconductor device adapted to prevent and/or thwart reverse engineering and a method for fabricating it according to the present invention is best depicted in Figure 2. The first embodiment according to the present invention is exemplified in Claims 1-8 and 17-18, which are allowed by the Examiner. As such, this embodiment and the associated claims are not the subject of this Appeal.

A second embodiment of a semiconductor device adapted to prevent and/or thwart reverse engineering and a method of for fabricating it according to the present invention is best depicted in Figure 3. The second embodiment according to the present invention is exemplified in Claims 9-16, 19-20 and 23-24. Because Claims 23-24 were found to be patentable, they are also not subject of this Appeal.

Referring to Figures 1 and 1(b), the semiconductor devices contain transistors that typically comprise a source 1, a drain 2, a gate 3 and field oxide layers 4. The semiconductor devices may further contain metallization 10 that is connected to the source 1 or drain 2 of the transistor though a metal plug 7. Typically, the reverse engineer looking at the metal plug 7 assumes that metallization 10 connected to the metal plug 7 is connected to either source 1 or drain 2 and

determines the functionality of the semiconductor device based on that connection. Referring to Figure 3, by providing metal plugs 7 that are not electrically connected to either source 1 or drain 2 of the transistor (i.e. contact region 9), the reverse engineer would wrongfully conclude that there is a connection to the contact region 9, which would lead to the wrong conclusion as to the functionality of the semiconductor device. This may be accomplished by disposing a metal plug 7 above a field oxide layer 4 instead of the contact region 9, as disclosed in the second embodiment of the present invention. See Figure 3 of the specification.

In summary, referring to Figure 3, by utilizing metal plugs 7 that are not electrically connected to the contact region 9 of the transistor the present invention is intended to prevent and/or thwart reverse engineering of the semiconductor devices by forcing the potential reverse engineer to examine every metallization 10 within the semiconductor device, which would require a lot of time and money there by making the reverse engineering of the integrated circuit prohibitive.

Overview of independent Claims 9 and 13

The embodiment of a semiconductor device adapted to prevent and/or thwart reverse engineering and a method of for fabricating it is exemplified in independent Claims 9 and 13.

Independent Claim 9 claims a semiconducting device adapted to prevent and/or to thwart reverse engineering, comprising: (a) field oxide layer disposed on a semiconductor substrate; (b) a metal plug contact disposed outside a contact region and above said field oxide layer, wherein said metal plug contact is electrically isolated from said contact region; and (c) a metal connected to said metal plug contact.

Independent Claim 13 claims a method for preventing and/or thwarting reverse engineering, comprising steps of: (a) providing a field oxide layer disposed on a semiconductor substrate; (b)

providing a metal plug contact disposed outside a contact region and above said field oxide layer, wherein said metal plug contact is electrically isolated from said contact region; and (c) connecting a metal to said metal plug contact.

Overview of dependent Claims 10-12, 14-16, 19-20 and 23-24

Claim 10 depends on Claim 9. Dependent Claim 10 recites that the semiconducting device of Claim 9 comprises integrated circuits.

Claim 11 depends on Claim 9. Dependent Claim 11 recites that the field oxide layer of Claim 9 comprises silicon oxide.

Claim 12 depends on Claim 10. Dependent Claim 12 recites that the integrated circuits of Claim 10 comprise complementary metal oxide-semiconductor integrated circuits and bipolar silicon-based integrated circuits.

Claim 14 depends on Claim 13. Dependent Claim 14 recites that the semiconducting device of Claim 13 comprises integrated circuits.

Claim 15 depends on Claim 13. Dependent Claim 15 recites that the field oxide layer of Claim 13 comprises silicon oxide.

Claim 16 depends on Claim 14. Dependent Claim 16 recites that the integrated circuits of Claim 14 comprise complementary metal oxide-semiconductor integrated circuits.

Claim 19 depends on Claim 9. Dependent Claim 19 recites that the field oxide layer of Claim 9 has an uppermost side, said metal plug contact being disposed on said uppermost side of said field oxide layer.

Claim 20 depends on Claim 13. Dependent Claim 20 recites that the field oxide layer of Claim 13 has an uppermost side, said metal plug contact being disposed on said uppermost side of said field oxide layer.

Claim 23 depends on Claim 9. Dependent Claim 23 recites that the metal plug contact of Claim 9 contacts said field oxide layer.

Claim 24 depends on Claim 13. Dependent Claim 24 recites that the metal plug contact of Claim 13 contacts said field oxide layer.

ISSUES

Issue 1:Whether Claims 9-16 and 19-20 are patentable under 35 U.S.C. 102(e) over Lee et al., U.S. Patent No. 6,255,155 (hereinafter "Lee")?

GROUPING OF CLAIMS

For each ground of rejection which the Applicants contest herein and which applies to more than one claim, such additional claims, to the extent separately identified and argued below, do not stand or fall together.

THE ARGUMENT

Issue 1: Whether Claims 9-16 and 19-20 are patentable under 35 U.S.C. 102(e) over Lee?

In the Office Action of July 15, 2004, the Examiner rejects Claims 9-16 and 19-20 under 35 U.S.C. 102(e) as being anticipated by Lee. Applicants respectfully disagree with the conclusions that the Examiner has made with regard to the teaching of the cited prior art and submit that Lee does not teach, disclose or suggest all of the claim limitations of the rejected claims. Applicants respectfully note that "[a] claim is anticipated only if each and every element as set forth in the clam is found, either expressly or inherently described, in a single prior art reference." MPEP 2131 quoting *Verdegaal Bros. V. Union Oil Co, of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Applicants also note that "[the] identical invention must be shown in as complete detail as is contained in the ... claim." MPEP 2131 quoting *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Applicants submit that the Examiner has not shown that Lee teaches each and every element as set forth in the rejected claims and the rejection based on Lee should be overturned on appeal.

Now the rejection of the specific claims by the Examiner based on the disclosure of Lee will be addressed.

Claims 9 and 13

Regarding Claims 9 and 13, the Examiner asserts, in part, that Lee's Figure 8 discloses "a semiconductor device adapted to prevent and/or thwart reverse engineering ... [and] a method for preventing and/or thwarting reverse engineering." The Examiner further asserts, in part, that Lee's Figure 8 discloses "a metal plug contact 42 disposed outside a

contact region 38b and above said field oxide layer, wherein said metal plug contact is electrically isolated from said contact region" as recited in Claims 9 and 13.

Applicants submit that the Examiner has not shown that Lee teaches, discloses, or suggests "a semiconductor device adapted to prevent and/or thwart reverse engineering ... [and] a method for preventing and/or thwarting reverse engineering." Applicants note that the Examiner has not cited any specific portion of Lee that provides the alleged teaching of "a semiconductor device adapted to prevent and/or thwart reverse engineering ... [and] a method for preventing and/or thwarting reverse engineering." Applicants further note that a word search of the Lee patent document as presented at the USPTO web site showed no matches for the words "reverse" or "engineering." How can Lee teach "a semiconductor device adapted to prevent and/or thwart reverse engineering ... [and] a method for preventing and/or thwarting reverse engineering" when the term "reverse engineering" is not even found in the Lee patent?

As to Examiner's assertion that the Examiner can overlook preamble limitations, it is submitted that the Examiner's assertion is not well taken. Indeed, the Court of Appeals for the Federal Circuit has said otherwise. See, for example, Corning Glass Works v. Sumitomo Elec. USA, Inc., 9 USPQ2d 1962 (Fed. Cir. 1989) and Catalina Mktg. Int'l v. Coolsavings.com 62 USPQ2d 1781 (Fed. Cir. 2002). Note, in particular, the following test set forth by the Court in the case of Catalina Mktg.:

> "No litmus test defines when a preamble limits claim scope...Some guideposts, however, have emerged from various cases discussing the preamble's effect on claim scope. For example, this court has held that Jepson claiming generally indicates intent to use the preamble to define the claimed invention, thereby limiting claim scope...Additionally dependence on a particular disputed preamble phrase for antecedent basis may limit claim scope ... Likewise when the preamble is essential to understand limitations or terms in the claim body ... Further when reciting additional structure or steps underscored as important by the specification, the preamble may operate as a claim limitation...Moreover, clear reliance on the preamble

> during prosecution to distinguish the claimed invention from the prior art transforms the preamble into a claim limitation ... Without such reliance, however, a preamble generally is not limiting when the claim body describes a structurally complete invention such that deletion of the preamble does not affect the structure or steps of the claimed invention."

The position being taken by the Examiner is clearly at odds with the Federal Circuit. Hence, Lee does not teach, disclose or suggest "a semiconductor device adapted to prevent and/or thwart reverse engineering" as recited in Claim 9 and "a method for preventing and/or thwarting reverse engineering" as recited in Claim 13.

The Applicants further submit that Lee does not teach "a metal plug contact disposed outside a contact region and above said field oxide layer, wherein said metal plug contact is electrically isolated from said contact region" (emphasis added) as recited in Claims 9 and 13.

The Examiner cites Figure 8 as disclosing "a metal plug contact 42 disposed outside a contact region 38b and above said field oxide layer, wherein said metal plug contact is electrically isolated from said contact region." However, the Applicants note that Figure 8 presents a cross-section along line II-II of the structure shown in Figure 6. A proper interpretation of the teachings of Lee requires an evaluation of Figures 6, 7, 8, 9a-9d, and 10a-10c and the associated text in the Lee specification. As will be seen the issue here is whether or not Lee meets the "electrically isolated" limitation found in Claims 9 and 13.

Lee defines region 38a as a source region and region 38b as a drain region in the active region of the substrate 31. See column 5, lines 65 – 67 of Lee. As such, one skilled in the art would understand the source region 38a to be electrically connected to the drain region 38b, since the movement of electrons between those two regions is required for the transistor defined by the source and drain regions to operate. Lee further states that metal pattern 43 is formed on the

tungsten plug 42. See column 6, lines 10 - 12. So, it may also be concluded that the tungsten plug 42 is in electrical contact with metal pattern 43.

In the Response to the Arguments section of the Office Action dated July 15, 2004, the Examiner asserts that "metal plug contact 42 is only connected with the gate electrode 35a and electrically isolated from said contact region 38b by the insulating layer 39." Applicants submit that this assertion contradicts the teachings of Lee. Lee states at column 6, lines 21 - 25:

> ". . . and there is a metal contact 43 connected to the cell transistors in common through a common source contact region in the extended source region 38a. The metal contact 43 connected to the common source contact region has a line form in a direction crossing the control gate 37a." (Underlining added for emphasis)

Therefore, Applicants submit that Lee teaches that the metal pattern 43 is electrically connected to the source region. Further, since the metal plug 42 is in electrical contact with the metal pattern 43, the metal plug 42 is in electrical contact with the source region 38a. Finally, since the source region 38a is in electrical contact with the drain region 38b, as discussed above, the metal plug 42 is in electrical contact with the drain region 38b and gate electrode 35a.

The Examiner seems to misunderstand the technology employed in teachings of Lee by believing that a gate structure is "electrically isolated" from the source and drain structures which it controls. Although the two may be physically separated, they are hardly "electrically isolated" from one another. Indeed, what happens (in terms of electrical potential) on the gate has a lot to do with what happens in the source and drain regions in terms of conduction therebetween.

According to the Examiner's analysis, if a Field Effect Transistor (FET) were placed in the Examiner's hands, the Examiner would say that the gate, drain and source electrodes are all "electrically isolated" from one another. To be consistent, the Examiner would also have to take the position that the electrodes of a capacitor are "electrically isolated" from one other. But, if

that were really true, why do electrical engineers even bother to put capacitors and FET transistors into circuits? The reason is that the electrodes of a capacitor are not "electrically isolated" from one another nor are the source, drain and gate electrodes of FET transistors "electrically isolated" from one another. It is exactly because they are not "electrically isolated" from each other that these devices provide useful functions in circuits.

As indicated in the Affidavit dated November 12, 2004, the Examiner appears to use a simplistic direct current (DC) analysis when taking the position that a gate of a FET device is electrically isolated from its associated drain. At DC, the resistance may well be infinite. However, since FET devices are normally used in alternating current applications, those skilled in the art know very well that FET devices can and will respond to the signals provided at the gates thereof. As such, the gates are hardly "electrically isolated" from the rest of the structure of the device, be it the drain or the source, as asserted by the Examiner. The impedance is anything but infinite. So, while there may be no DC connection between a gate and either the source or drain of an FET transistor, that does not imply that the gate is electrically isolated from the drain or the source. Indeed, that which happens at the gate directly influences that which happens at the source and drain of a FET device and therefore the gate of a FET device is not electrically isolated from either its source or its drain.

As indicated in the Affidavit dated November 12, 2004, the Examiner's assertions seem to fly in the face of common knowledge in the electrical arts. The Examiner failed to provide any evidence to support his beliefs, which Applicants believe are unorthodox, even when Applicants called upon the Examiner to cite some reference supporting his views. The Examiner also failed to comply with the rules of practice, particularly 37 C.F.R. 1.104(d)(2) and supply the Affidavit specifically setting forth the "facts" upon which he relies in rejecting Claims 9 and 13.

Hence, the Applicants submit that Lee does not teach "said metal plug contact is electrically isolated from said contact region" (emphasis added) as claimed in Claims 9 and 13. Instead, the Applicants submit that Lee teaches that the metal plug contact is electrically connected to the contact region, as defined by the Examiner. Therefore, the Applicants submit that the Examiner has not shown that Lee teaches each and every element as set forth in Claims 9, 13 and Claims 9, 13 are patentable over Lee.

Claims 10-11

Regarding Claims 10-11, the Applicants submit that Claims 10-11 are patentable over Lee at least based upon their dependence on Claim 9.

Claim 12

Regarding Claim 12, the Examiner asserts, in part, that Lee discloses on Figure 8 "said integrated circuits further comprise complementary metal oxide semiconductor integrated circuits and bipolar silicon based integrated circuits." See page 3 of the Office Action dated July 15, 2004.

Applicants submit that the Examiner failed to comply with 37 C.F.R. §1.104(c)(2) which states:

> "In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command. When a reference is complex or shows or describes invention other than that claimed by Applicant, **the particular part relied on must be designated as nearly as practicable**. The pertinence, if not apparent, must be clearly explained and each rejected claim specified" (emphases added).

Applicants submit that the Examiner has failed to "designate as nearly as practicable" the particular part of Lee relied upon in making the assertion that Lee teaches "said integrated circuits further comprise complementary metal oxide-semiconductor integrated circuits and

bipolar silicon-based integrated circuits" as recited in Claim 12. Therefore, the Applicants submit that the Examiner has not shown that Lee teaches each and every element as set forth in Claim 12 and Claim 12 is patentable over Lee.

Claims 14-16

Regarding Claims 14-16, the Applicants submit that Claims 14-16 are patentable over Lee at least based upon their dependence on Claim 13.

Claims 19-20

Regarding Claims 19 and 20, the Applicants submit that Claims 19 and 20 are patentable over Lee at least based upon their dependence on Claims 9 and 13, respectively. Further, the Applicants submit that the Examiner has not shown that Lee teaches, discloses, or suggests "said metal plug contact being disposed on said uppermost side of said field oxide layer" as recited in Claims 19 and 20.

The Examiner asserts that "metal plug" as recited in Claims 19 and 20 is disclosed by Lee's plug "42." According to Lee, The Examiner further asserts that the "field oxide layer" as recited in Claims 19 and 20 is disclosed by Lee's oxide film "33." The Examiner also asserts that Lee's Figure 8 discloses plug "42" being disposed on the uppermost side of the oxide film "33."

The Examiner appears to misunderstand the teaching of Lee. Contrary to the Examiner's assertions, Applicants submit that Lee does not teach, disclose or suggest "said metal plug contact being disposed on said uppermost side of said field oxide layer" as recited in Claims 19 and 20. Applicants respectfully submit that Lee discloses a plug "42" disposed on polysilicon layer "35," not oxide film "33" as asserted by the Examiner. See

Figure 8 of Lee. Because plug "42" as disclosed by Lee is disposed on polysilicon layer "35," how can it be disposed on the oxide film "33"? Hence, Lee does not teach, disclose, or suggest "said metal plug contact being disposed on said uppermost side of said field oxide layer" (emphasis added) as recited in Claims 19 and 20 and Claims 19 and 20 are patentable over Lee.

Conclusion

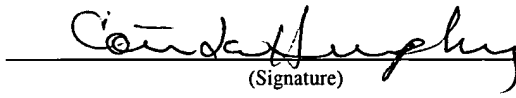
For the extensive reasons advanced above, Appellant respectfully contends that each claim is patentable. Therefore, reversal of all rejections and objections is courteously solicited.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account no. 12-0415. In particular, if this Appeal Brief is not timely filed, the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being deposited with the United States Post Office with sufficient postage as express mail in an envelope addressed to: Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22323-1450 on

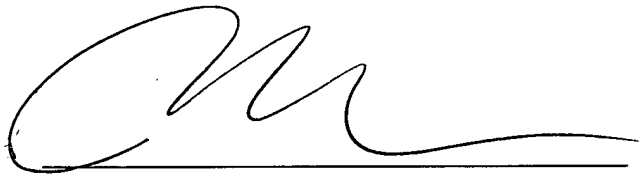
February 24, 2005
(Date of Mailing)

Corinda Humphrey
(Name of Person Mailing)


(Signature)

February 24, 2005
(Date)

Respectfully submitted,



Richard P. Berg
Attorney for Applicant
Reg. No. 28,145
LADAS & PARRY
5670 Wilshire Boulevard, Suite 2100
Los Angeles, California 90036
(323) 934-2300

1. (Previously Presented) A semiconducting device adapted to prevent and/or to thwart reverse engineering, comprising:

(a) field oxide layer disposed on a semiconductor substrate and within a contact region;

(b) a metal plug contact disposed within said contact region and above said field oxide layer, wherein said metal plug contact contacts said field oxide layer, and wherein said field oxide layer electrically isolates said metal plug contact from said contact region; and

(c) a metal connected to said metal plug contact.

2. (Original) The device as claimed in claim 1, wherein said semiconducting device comprises integrated circuits.

3. (Original) The device as claimed in claim 1, wherein said field oxide layer further comprises silicon oxide.

4. (Original) The device as claimed in claim 2, wherein said integrated circuits further comprise complementary metal oxide-semiconductor integrated circuits and bipolar silicon-based integrated circuits.

5. (Previously Presented) A method for preventing and/or thwarting reverse engineering, comprising steps of:

(a) providing a field oxide layer disposed on a semiconductor substrate and within a contact region;

(b) providing a metal plug contact disposed within said contact region and above said field oxide layer, wherein said metal plug contact contacts said field oxide layer, and wherein said field oxide layer electrically isolates said metal plug contact from said contact region; and

(c) connecting a metal to said metal plug contact.

6. (Original) The method as claimed in claim 5, wherein said semiconducting device comprises integrated circuits.

7. (Original) The method as claimed in claim 5, wherein said field oxide layer further comprises silicon oxide.

8. (Original) The method as claimed in claim 6, wherein said integrated circuits further comprise complementary metal oxide-semiconductor integrated circuits.

9. (Previously Presented) A semiconducting device adapted to prevent and/or to thwart reverse engineering, comprising:
(a) field oxide layer disposed on a semiconductor substrate;
(b) a metal plug contact disposed outside a contact region and above said field oxide layer, wherein said metal plug contact is electrically isolated from said contact region; and
(c) a metal connected to said metal plug contact.

10. (Original) The device as claimed in claim 9, wherein said semiconducting device comprises integrated circuits.

11. (Original) The device as claimed in claim 9, wherein said field oxide layer further comprises silicon oxide.

12. (Original) The device as claimed in claim 10, wherein said integrated circuits further comprise complementary metal oxide-semiconductor integrated circuits and bipolar silicon-based integrated circuits.

13. (Previously Presented) A method for preventing and/or thwarting reverse engineering,

comprising steps of:

(a) providing a field oxide layer disposed on a semiconductor substrate;

(b) providing a metal plug contact disposed outside a contact region and above said field oxide layer, wherein said metal plug contact is electrically isolated from said contact region; and

(c) connecting a metal to said metal plug contact.

14. (Original) The method as claimed in claim 13, wherein said semiconducting device comprises integrated circuits.

15. (Original) The method as claimed in claim 13, wherein said field oxide layer further comprises silicon oxide.

16. (Original) The method as claimed in claim 14, wherein said integrated circuits further comprise complementary metal oxide-semiconductor integrated circuits.

17. (Previously Presented) The device as claimed in claim 1, wherein said field oxide layer has an uppermost side, said metal plug contact being disposed on said uppermost side of said field oxide layer.

18. (Previously Presented) The method as claimed in claim 5, wherein said field oxide layer has an uppermost side, said metal plug contact being disposed on said uppermost side of said field oxide layer.

19. (Previously Presented) The device as claimed in claim 9, wherein said field oxide layer has an uppermost side, said metal plug contact being disposed on said uppermost side of said field oxide layer.

20. (Previously Presented) The method as claimed in claim 13, wherein said field oxide layer has an uppermost side, said metal plug contact being disposed on said uppermost side of said field

oxide layer.

21. (Canceled)

22. (Canceled)

23. (Previously Presented) The device of claim 9, wherein said metal plug contact contacts said field oxide layer.

24. (Previously Presented) The method of claim 13, wherein said metal plug contact contacts said field oxide layer.